VERSION WITH MARKINGS TO SHOW CHANGES MADE

On page 2, delete lines 24-25.

Amend page 2, line 26 as follows:

Figures [8A-8D] 7A-7D are block diagrams of components employed in digital realizations of components of the invention.

Amend page 7, paragraph 34 as follows:

[Referring now to Figure 7, t] The cancellation circuit 36 is illustrated. Its purpose in this context is to take a replica of the modulated signal which has been compensated for upconverter-introduced errors and compare it with a downconverter-compensated received signal and remove the component of that received signal due to the user's own transmission, including upconverter introduced errors. The cancellation circuit 36 finds application in self-interference removal systems employing replica signal generation. The cancellation circuit employs time and phase detectors [250] to correlate the two complex input signals to generate signals to drive phase and time tracking loops [252, 254] that control delay and modulation elements 30, 32. The control of time and phase allow the replica signal to align with that portion of the composite relayed signal attributable to the user's own transmissions (i.e., the user's relayed signal). The replica modulator outputs [253, 255] are provided to an adaptive filter [256]. The adaptive filter [256] mimics the linear effects that the user's relayed signal has encountered in the transmission channels via the relay 22. These effects will be present at the output of the receive compensator 12. A summer [258] removes the user-originated signal from the composite signal.

Amend page 8, paragraph 36 as follows:

A number of techniques can be used to implement the structures of Figure 4, Figure 5 and Figure 6. Some representative examples are illustrated in Figures [8A-8D] 7A-7D. The outputs of the downconverter 34 can be digitized (through analog to digital converters not shown) so that all subsequent processing can be in the digital

domain. The errors introduced by upconversion and downconversion are artifacts of analog processing.

Amend page 8, paragraph 37 as follows:

Referring to Figure [8A] 7A, the DC filters 102, 104, 202, 204 can be realized digitally as a sign detector 302 followed by a counter 304. Each positive sample increments the counter, while each negative sample decrements the counter. If there is no DC component in the digital representation of the incoming signal, then the long term average of the counter output will be zero. If there is a DC component, however, the value of the counter will go positive or negative to reflect that value. In the application of interest, once the DC value of the incoming signal is achieved at the output of the counter, then the input to the sign detector will have zero DC, and the system will stabilize. The precision of the counter affects the speed of this convergence and the sensitivity to noise.

Amend page 8, paragraph 38 as follows:

In a similar fashion, referring to Figure [8B] 7B, the phase comparators 112, 212 can be implemented by a correlator fashioned by a multiplier 306 multiplying the signs (elements 308, 310) of the I and Q branches together. In practice, this is accomplished by comparing the sign bits. If the two sign bits are the same, then the output would be +1, while if they differ, the output would be the inverse or -1. The same correlator structure of Figure 8B is used for the correlator of element 314 (Figure 6).

Amend page 8, paragraph 39 as follows:

The magnitude comparators 114, 214 can also be implemented with a sign detector arrangement (Figure [8C] 7C). The input to the sign detector is the difference in amplitudes (absolute values) of the I path signal and the Q path signal.

Amend page 8, paragraph 40 as follows:

The filters 118, 122, 218, 222 can be implemented by an up/down counter (Figure [8D] 7D) that increments for positive values and decrements for negative values.